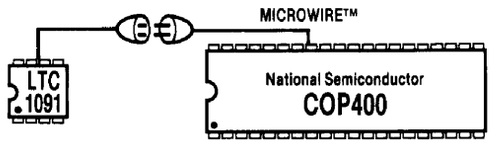
Interfacing the LTC1091 to the COP402N MCU



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Introduction

This application note describes the hardware and software required for communication between the LTC1091 10-bit data acquisition system and the National Semiconductor COP400 microcontroller family which uses the MICROWIRE serial interface. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data in 116μs. Configuration of the LTC1091 and the COP402N will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1091 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a half duplex format over D_{IN} and D_{OUT}.

The National Semiconductor MICROWIRE interface is a synchronous, full duplex, serial port built into the COP400 family that allows the user to easily interface to the LTC1091. MICROWIRE provides clock, data in and data out lines that are compatible with the LTC1091. One additional line (G0) is required to control the $\overline{CS}$ pin on the LTC1091. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The actual interface will involve using the COP402N, a member of the COP400 family. All code shown here should work with any of the COP400 family.

The code for this interface was developed on a COP400 evaluation board which allows an external EPROM to be used in place of the internal processor ROM.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer. The COP402N clock was 4MHz.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

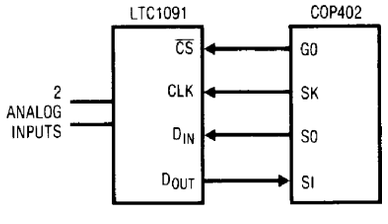


Figure 1. Schematic

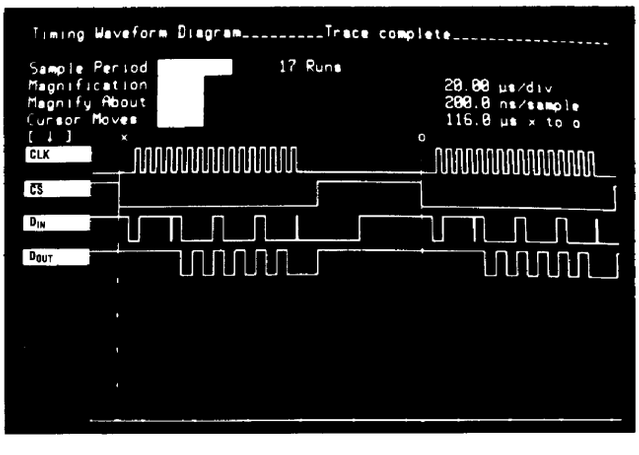


Figure 2. Timing Diagram

Software Description

The software configures and controls the MICROWIRE serial interface of the COP402N. Additionally, the software manipulates G0 ($\overline{CS}$ of the LTC1091).

The code first initializes the B register and then loads the LTC1091 D_{IN} word into the RAM of the COP402 one nibble at a time. As shown in Figure 3 the D_{IN} word configures the LTC1091 for CH1 with respect to GND and MSB first. SO is configured as an output. The carry is set so that when an XAS instruction is generated the shift clock (SK) will begin clocking data.

The first nibble of the D_{IN} word is loaded into the ACC and G0 ($\overline{CS}$) is cleared. The D_{IN} nibble is loaded into the shift register and the data begins to shift. The second nibble of the D_{IN} word is loaded into the ACC. One NOP is allowed for timing and then the contents of the ACC are swapped with those of the shift register. The transfer continues. One NOP is allowed for timing. The second D_{IN} nibble is loaded into the ACC again and the contents of the ACC are swapped with those of the shift register. The MSBs of the LTC1091 D_{OUT} word are now in the ACC. This data is then stored in memory location $13. The ACC is loaded with the second D_{IN} nibble from RAM and another swap

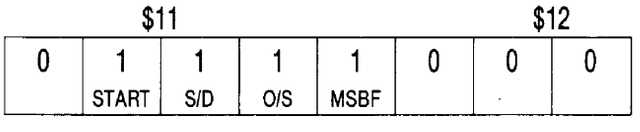
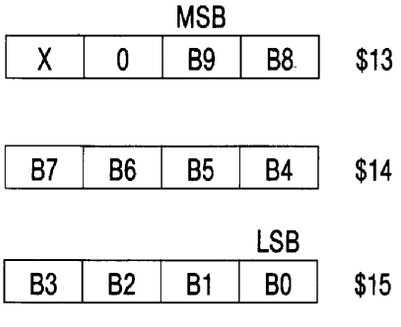


Figure 3. D_{IN} Word for LTC1090



D_{OUT} from LTC1091 stored in COP402 RAM

Figure 4. Memory Map

LABEL	MNEMONIC		COMMENTS
	CLRA		MUST BE FIRST INSTRUCTION
	LBI	1,1	BR = 1 BD = 1 INITIALIZE B REG.
	STII	7	FIRST D_{IN} NIBBLE IN $11
	STII	8	SECOND D_{IN} NIBBLE IN $12
	LEI	8	SET EN TO (1000) BIN
	SC		CARRY SET
	LDD	1,1	LOAD FIRST D_{IN} NIBBLE IN ACC
	OGI	50	G0 ($\overline{CS}$) CLEARED
	XAS		ACC TO SHIFT REG. BEGIN SHIFT
	LDD	1,2	LOAD NEXT D_{IN} NIBBLE IN ACC
	NOP		TIMING
	XAS		NEXT NIBBLE, SHIFT CONTINUES
	NOP		TIMING
	LDD	1,2	LOAD NULL DATA IN ACC
	XAS		NEXT NIBBLE, SHIFT CONTINUES
	XIS	0	FIRST NIBBLE D_{OUT} TO $13
	LDD	1,2	LOAD NULL DATA IN ACC
	XAS		SHIFT CONTINUES, $D_{OUT} \rightarrow$ ACC
	XIS	0	NEXT NIBBLE D_{OUT} TO $14
	RC		CLEAR CARRY
	CLRA		CLEAR ACC
	XAS		THIRD NIBBLE D_{OUT} TO ACC
	OGI	51	G0 ($\overline{CS}$) SET
	XIS	0	THIRD NIBBLE D_{OUT} TO $15
	LBI	1,3	SET B REG. FOR NEXT LOOP

Figure 5. COP402 Code

between the ACC and the shift register is executed. The next D_{OUT} nibble is stored in $14. The carry is cleared so that on the next XAS instruction the shift clock will stop. The XAS instruction is executed and the final nibble of the LTC1091 D_{OUT} word containing the LSBs is loaded into the ACC. G0 ($\overline{CS}$) is taken high. The third D_{OUT} nibble is stored in location $15. The B register is then reinitialized so that when the loop is run again the data will always be stored in the same memory locations. The D_{OUT} data from the LTC1091 is now in a right justified format as shown in Figure 4.

Summary

A four wire interface between the LTC1091 and the COP402N with a combined data conversion and transfer time of 116μs was demonstrated. The interface used the MICROWIRE serial port of the COP402N. The 10 data bits of the LTC1091 are shifted MSB first in four four bit transfers. The data is stored right justified in the COP402N's internal RAM. The code demonstrated will work on any member of the COP400 family.

MICROWIRE is a trademark of National Semiconductor Corp.